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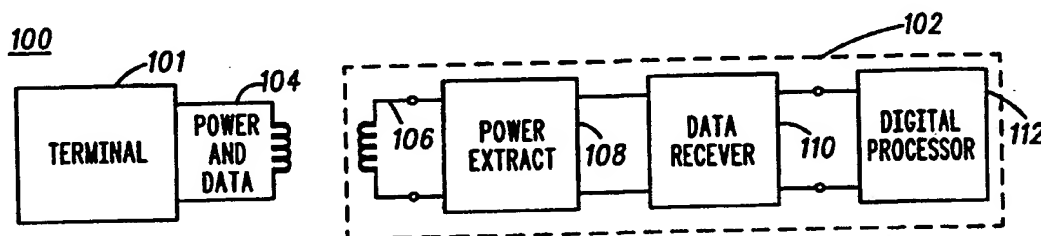
(57) Abstract

A portable data device (102) employs a single coil (106) for receiving both power and data from a terminal (101) and includes a power rectifier (205) and an ASK data receiver (215). A shunt regulator circuit (211) is coupled between the power rectifier (205) and the ASK data receiver (215) and is used to control a mode selector (203). The mode selector (203) is used for switching between a power extraction mode of operation and a data exchange mode of operation.

PORTABLE DATA DEVICE AND METHOD OF SWITCHING BETWEEN A
POWER AND DATA MODE OF OPERATION

Field of the Invention

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The invention relates generally to portable data devices and a method for switching between two modes of operation thereof.

Background of the Invention

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Data transmission systems are known to include terminal devices (sometimes called readers or exciters) and portable data devices (sometimes called cards or smartcards). It is well understood that today's portable data devices include memory and processor devices require power from the terminal device. Once such a portable device (which may be contactless or contacted/contactless -- sometimes referred to as combicards) enters into the excitation field of the terminal device, power and data can thereafter be transferred from the terminal device to the portable data device. Historically, portable data devices have been designed using two antenna structures; one for receiving power and a second for receiving/transmitting data. More recently, designs have focused on having a single antenna structure that is designed to receive power and data from the terminal device. (It should be noted that these antenna structures are commonly made of inductive coils, and such single antenna devices are commonly referred to as single coil cards.) Of course, reducing the number of antennas has the effect of introducing related circuit problems and design challenges.

These problems include 1) providing effective power regulation while allowing for data reception; and 2) providing noise isolation and

discrimination from the digital elements within the portable data device. The coil, in a single coil portable data device, serves as the power and signal reception element through which power and data signaling is delivered to the card. The power extraction and regulation circuitry

5   regulates and delivers power from the coil while allowing the data signal to coexist on top of the regulated power. The regulated power is used by all circuitry on the portable data device. The receiver couples the data signal from the regulated power and transforms it to digital levels that can be further processed by the digital circuitry.

10   The design of a receiver that optimizes power reception while still being able to accurately detect amplitude shift keying (ASK) modulated data can be rather complex. Moreover, such circuits typically induce significant delays in the transaction, as the circuit must essentially be re-configured to receive data after the power signal is initially extracted.

15   Of course, the timing requirements for today's so-called smart cards is such that long transaction times are undesirable, particularly during a secure application, such as a credit/debit transaction. Accordingly, there exists a need for a single coil portable data device that is not constrained by the shortcomings of the prior art. In particular, a card

20   architecture that allowed for timely switching between a power extraction mode of operation and a data receiving mode of operation would be an improvement over the prior art. Moreover, such a portable data device that used less complex circuitry would provide a further advancement of the prior art.

25

Brief Description of the Drawings

FIG. 1 shows a data transmission system that includes a terminal device and a portable data device, in accordance with the present invention;

FIG. 2 shows a more detailed view of the portable data device shown in FIG. 1;

FIG. 3 shows a more detailed diagram of the shunt regulator circuit shown in FIG. 2;

FIG. 4 shows a more detailed schematic diagram of a circuit that includes the mode selector shown in FIG. 2;

FIG. 5 shows a more detailed circuit diagram of the ASK receiver circuit shown in FIG. 2;

FIG. 6 shows a more detailed schematic diagram of enhanced coupling circuit shown in FIG. 5; and

FIG. 7 shows a flow diagram depicting the mode selection operation, in accordance with the present invention.

Detailed Description of a Preferred Embodiment

The present invention encompasses a portable data device that includes a single coil for receiving both power and data from a terminal device. The portable data device further includes a power rectifier and a shunt regulator circuit, which act in concert to extract power from signals emitted by the terminal device. An amplitude shift keyed (ASK) data receiver is also included on the card to receive transmitted data signals and produce demodulated data. A mode selector is employed for switching between the power extraction mode of operation and the data mode of operation. By using the aforementioned components, the present invention allows for an efficient transition between a first mode, designed to receive power while performing tasks that generate

potentially disruptive noise, and a second mode, designed to receive data from the terminal device, as described herein.

FIG. 1 shows a data transmission system 100 that includes a terminal device 101 and a portable data device 102, in accordance with the present invention. Terminal 101 includes a transmission structure 104, which consists of a single coil for transmitting both power and data. Power and data is transmitted using a signal that is partially modulated with data, typically with a modulation index of 10%. A partially modulated signal provides an uninterrupted power source that is required by the more sophisticated portable data devices, or smart cards, that use microprocessors. The card 102 includes a single coil 106 for receiving power signals and data signals from the terminal 101. A power extractor 108 is employed to extract power for use by the analog and digital circuitry employed by the card, as later described. A data receiver 110 is used to receive and demodulate the data signals transmitted from the terminal 101. Digital processor 110 is used to manipulate the demodulated data and perform various functions thereon.

FIG. 2 shows a more detailed diagram of the portable data device 102 shown in FIG. 1. In accordance with a preferred embodiment of the invention, a shunt device 201, placed across the single coil 106, is controlled by a mode selector 203, as later described. The received signals are inputted to rectifier 205 to produce a rectified high voltage (Vdd) 207 and a rectified low voltage (Vss) 209. A shunt regulator circuit 211, which outputs a shunt control signal 213 as later described, is also employed by the card 102, in accordance with the invention. A data receiver 215, which in a preferred embodiment is an amplitude shift keyed (ASK) receiver, is employed by the card 102 to produce demodulated data 217. By using the shunt regulator circuit 211 and the mode selector 203, the present invention allows the card to switch between a power extraction mode that is highly dynamic and a power extraction mode that

allows for data to reside on top of the extracted power, as later described.

FIG. 3 shows a more detailed block diagram of the shunt regulator circuit 211 shown in FIG. 2. As shown, the shunt regulator circuit 211 consists of a reference voltage generator 302 and a differential comparison circuit 304. The reference voltage generator 302 generates a reference voltage for each of the corresponding nodes, Np and Nn. According to the invention, the voltage on node Np is referenced to Vdd and offset from Vdd to a lower potential value by a fixed amount. This offset voltage is set to one PMOS threshold voltage by using a PMOS device in a diode equivalent configuration (i.e., gate connected to the drain). Similarly, the voltage on node Nn is referenced to Vss and offset from Vss to a higher value by a fixed amount. This offset voltage is set to one NMOS threshold voltage by using a NMOS device in a diode equivalent configuration (i.e., gate connected to the drain). When the potential between Vss and Vdd is below its regulated value, the potential on Nn is higher than the potential on Np and the output of the comparison circuit is low. As Vdd rises in response to receiving more power, Np also rises by the same amount. Correspondingly, as Vss goes lower, in response to receiving more power, Nn also goes lower by the same amount. This phenomenon is used to effectively determine when the power is at an acceptable level, while still maintaining a level of receive sensitivity to accurately detect data, in accordance with the invention.

At a predetermined power level, the rising potential on Np becomes higher than the falling potential on Nn, and as a result the differential comparison signal 213 begins to rise. As the output level of differential comparison signal 213 rises, it turns on the shunt device 201, which in turn shunts a portion of the received power across the coil 106. The gain of the differential comparison circuit is kept low so that it does not overdrive the NMOS shunt device. Typically, the shunt device is of the

NMOS type on a P-substrate, which results in a more efficient structure without any additional semiconductor wells that can potentially cause a fatal condition commonly referred to as "latch-up." If the rectified power continues to rise, in response to receiving more power on the coil

5   (e.g., the card is brought very close to the terminal), the potential difference between Vdd and Vss (and correspondingly between Np and Nn) becomes larger. The larger potential between Np and Nn results in the comparison circuit 304 providing more drive to the shunt device 201. The increased drive results in element 201 shunting most of the increased

10   power across the coil, thus maintaining the rectified voltage within the operational range of the smart card chip.

As shown and described, the reference voltage generator 302 develops a differential pair of voltage references (i.e., on nodes Np and Nn) to enhance the overall noise discrimination properties of the voltage

15   regulator. In accordance with the invention, these two reference voltages are generated using similar techniques so that noise coupled onto them has the same characteristics, and is therefor seen as so-called "common mode" by the differential comparison circuit 304. The differential comparison circuit 304 is designed to have a high common mode rejection

20   capability and therefore does not react to any common mode signals.

FIG. 4 shows a more detailed view of the mode selector 203, as well as the shunt device 201, shown in FIG. 2. According to the invention, a time constant is derived from a resistive element 401 and the gate capacitance of the shunt device 201. This time constant determines the

25   delay characteristics between the input of the mode selector 203 and its output. When switch 403 is open, as shown, the time constant serves to delay any change in voltage from taking immediate effect at the gate of the shunt device 201. This mode is called the low dynamic mode or data receive mode, and accounts for why the simplified receiver configuration

can effectively detect data on top of the received power signal, according to the invention, as next described.

A data modulated power signal, received from the terminal device 101 (shown in FIG. 1), results in a rectified DC power signal that has a
5   differential data component. The differential data component consists of a signal that changes in opposing directions between nodes Vdd and Vss. If the received power signal increases in amplitude, in response to a modulated logic "1" being transmitted, the differential data component on Vdd and Vss causes Vdd and Vss to diverge from each other. Conversely,
10 when the received power signal is reduced in amplitude, in response to a modulated logic "0", Vdd and Vss converge toward each other.

When data is to be received, the resident processor (e.g., microprocessor or microcontroller, not shown) sends a switch control signal 214 to open switch 403. This higher impedance path selection
15 results in a delay of the differential comparison signal 213 being applied to the shunt device 201. This in turn delays the shunt device from responding and eliminating the amplitude change on Vdd and Vss, thereby allowing the data to exist on Vdd and Vss during and shortly after data transitions. When the differential signal between Vdd and Vss is no
20 longer in transition, the drive to the shunt device returns to the same potential as the differential comparison signal 213 (i.e., after the delay as determined by the time constant). In this manner, data can be effectively received using relatively simple circuitry, as contrasted with the receiver circuits of the prior art, as later described.

25   Of course, when the switch 403 is closed across resistor 401, the time constant is reduced to zero and the low impedance drive of the differential comparison circuit 304 dominates the voltage seen at the gate of the shunt device 201. This mode is selected when the objective is to receive power at an optimum level (e.g., when the card first enters the
30 field of the terminal) and is referred to as the high dynamic mode . In this

mode, any change in the voltage difference between Vdd and Vss is immediately reflected in a change in the drive level to the shunt device 201, resulting in the change being eliminated. It is well understood that changes in the potential difference can be caused by the loading level of

5   the internal power bus, transient switching noise, movements of the portable data device relative to the terminal device or an amplitude difference in the received power signal caused by ASK modulated data. Accordingly, the portable data device 102 conducts a majority of its digital operations while in this mode, so that detected power fluctuations

10 are effectively eliminated.

It should be noted that resistor 405 resolves an initialization condition that occurs when the portable data device 102 first enters the excitation field from the terminal device 101. The condition occurs as the rectified voltage between Vdd and Vss begins to build, but is still below

15 the operational level of the differential comparison circuit 304. Under this condition, no drive is being supplied from the differential comparison circuit 304, and thus, the only drive at the output of the mode selector 203 is through resistor 405. The drive through resistor 405 keeps shunt device 201 off until the rectified voltage is sufficient for the differential

20 comparison circuit to drive the mode selector circuit.

FIG. 5 shows a more detailed view of the receiver 215 shown in FIG. 2, in accordance with the invention. In a preferred embodiment, the ASK receiver consists of an enhanced coupling circuit 502, an intermediate amplification stage 504, a signal centering circuit 506 and a high-gain,

25 noise tolerant amplifier 508. The enhanced signal coupling circuit 502 couples the differential data signal from Vdd and Vss onto nodes I_N and I_{NB} . The intermediate amplification stage 504, and the signal centering circuit 506, amplifies and re-centers the differential data signal about a common reference voltage. According to the invention, the final amplifier

30 508 is a high-gain stage capable of boosting the data signal to digital

levels. Further, amplifier 508 provides a data-dependent hysteresis with respect to the re-centered differential input. The hysteresis characteristic provides some level of noise immunity and additionally serves to maintain a constant digital output level during long periods

5 where there are no data transitions.

FIG. 6 shows a more detailed view of the enhanced coupling circuit 502 shown in FIG. 5. As shown, capacitors C_b couple the differential data signal from Vss and Vdd onto nodes I_N and I_{NB}. To further enhance the AC coupled signal through capacitors C_b, a DC coupling component has been

10 added through resistors R1 and R2. Typically R1 and R2 values are chosen to couple the AC signal so that it can then be directly amplified. However, by making R1 substantially smaller than R2, an additional DC coupling component from Vdd and Vss is realized. The following equation identifies the additional DC signal coupling through resistors R1 and R2,

15 where ΔVdd and ΔVss represents the signal change on Vdd and Vss, respectively:

$$\text{DC coupling component} = 2 * \frac{(R2 - R1)}{(R1 + R2)} * (\Delta Vdd + \Delta Vss)$$

20 Of course, it can be seen that the DC coupling component is proportional to the difference in values of R2 and R1.

FIG. 7 shows a data flow diagram 700 depicting operation of the mode selection method of the present invention. Upon placing a card in the field (702), the power signal that is received by the card is rectified

25 (704). From this rectified power voltage, the two reference voltages Vdd and Vss are generated (706) and compared (708) to produce a differential comparison signal (213 shown in FIG. 2). The rectified power signal is then regulated (710) to arrive at a stable operating voltage level (e.g., 3 volts). This mode of power regulation is referred to herein as the power

30 extraction or high dynamic mode. This regulation step continues until it

is determined (712) that the microprocessor is being powered by a stable operating voltage. Upon stabilization, the processor then completes a majority of its digital operations in preparation for receiving data (713). The microprocessor then enters (714) the data mode, and is thereafter

5   able to exchange data with the terminal device 101 shown in FIG. 1. As part of entering this mode, the microprocessor sends a switch control signal 214 to the mode selector circuit 203 (both shown in FIG. 2) to open the switch 403 (shown in FIG. 4). At this point, the regulator enters (718) the data receive mode, referred to herein as the low dynamic mode.

10   The circuits presented in FIG.s 1 through 6 offer a unique but simple solution to the problems of effective power regulation and noise isolation for a single coil portable data device. According to the invention, power regulation is achieved through a noise discriminating regulator that supports two modes of operation. In a first mode, which is highly

15   dynamic, the portable data device conducts the majority of its digital operations so that power fluctuations caused by turning on and off large digital functions (and the corresponding switching noise caused by these functions) is effectively eliminated. In a second mode, which has a slower response time, both data and noise are allowed to coexist on Vdd

20   and Vss. To mitigate the noise problem, the portable data device curtails most of its digital operations while in this mode so that noise produced by turning on and off large digital functions (along with their associated switching noise) does not adversely affect the receiver.

Additionally, noise discrimination is achieved through the unique

25   architecture of the shunt regulator. According to the invention, this shunt regulator provides two reference voltages having similar characteristics, so that noise is seen and rejected as common mode at the inputs to the comparator circuit. Lastly, to enhance the amount of signal coupling from Vdd and Vss to the differential receiver, a unique coupling arrangement is

30   provided that maximizes the amount of both AC and DC signal coupling.

What is claimed is:

Claims

1.   A portable data device that includes a single coil, having a first and second terminal, for receiving both power and data from a terminal, the

5   portable data device comprising:

a power rectifier operably coupled to the single coil;

an ASK data receiver operably coupled to receive data transmitted from the terminal to the single coil;

a shunt regulator circuit operably coupled between the power

10   rectifier and the ASK data receiver; and

mode selector means, operably coupled to the shunt regulator circuit, for switching between a power extraction mode of operation and a data exchange mode of operation.

15   2.   The portable data device of claim 1, wherein the data transmitted by the terminal is modulated using a modulation index substantially less than 100%.

3.   The portable data device of claim 1, wherein the shunt regulator

20   circuit further comprises a reference voltage generator having a first output referenced to a rectified high voltage (Vdd) and a second output referenced to a rectified low voltage (Vss).

4.   The portable data device of claim 3, wherein the shunt regulator

25   circuit further comprises a differential comparison circuit operably coupled to the first and second outputs of the reference voltage generator, wherein the differential comparison circuit comprises a differential output that reflects a difference between the first and second reference outputs from the reference generator.

5.   The portable data device of claim 1, wherein the ASK data receiver further comprises an enhanced coupling circuit coupled to the power rectifier and having as inputs Vss and Vdd.

6.   A portable data device that includes a single coil, having a first and second terminal, for receiving both power and data from a terminal, the portable data device comprising a CMOS integrated circuit that includes:

a power rectifier operably coupled to the single coil;

5   an ASK data receiver operably coupled to receive modulated data transmitted from the terminal to the single coil using a modulation index in the range of 5% - 15%;

a shunt regulator circuit operably coupled between the power rectifier and the ASK data receiver; and

10   mode selector means, operably coupled to the shunt regulator circuit, for switching between a power extraction mode of operation and a data exchange mode of operation.

7.   The portable data device of claim 9, wherein the shunt regulator

15   circuit further comprises a reference voltage generator having a first output referenced to within one PMOS threshold voltage of a rectified high voltage (Vdd) and a second output referenced to within one NMOS threshold voltage of a rectified low voltage (Vss).

20

8   The portable data device of claim 10, wherein the shunt regulator circuit further comprises a differential comparison circuit operably coupled to the first and second outputs of the reference voltage generator, and wherein the differential comparison circuit comprises a low-gain

25   differential output that reflects a difference between the first and second reference outputs from the reference generator.

9.   The portable data device of claim 11, further comprising an NMOS shunt device operably coupled between the first and second terminal of

the single coil and having a control input operably coupled to the differential output.

10.   In a portable data device that includes a single coil having a first and second terminal for receiving both a power signal and a data signal from a terminal, a method of selecting between a power extraction mode of operation and a data exchange mode of operation, the method
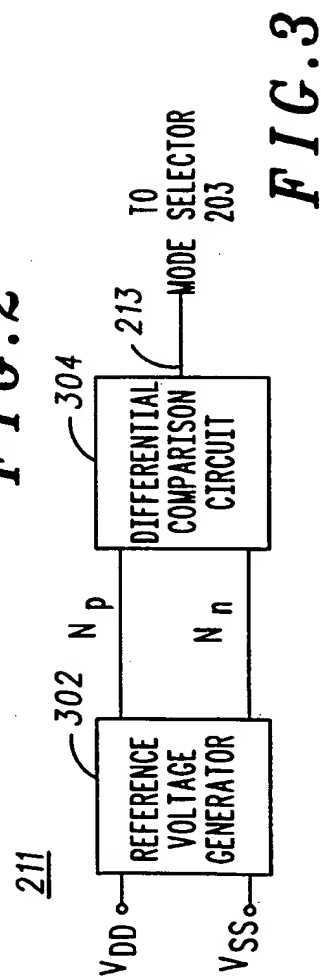
5   comprising the steps of:

rectifying the received power signal to thereby produce a rectified high voltage (Vdd) and a rectified low voltage (Vss);

generating a first and second reference voltage based at least in part on Vdd and Vss;

10   comparing the first and second reference voltages to produce a differential comparison signal at a first node, whereby the differential comparison signal serves to engage a shunt device, wherein the shunt device is disposed across the first and second terminals of the single coil; and

15   switching a resistive element between the first node and the shunt device, thereby switching between a power extraction mode of operation and a data exchange mode of operation.

FIG.1

FIG.2
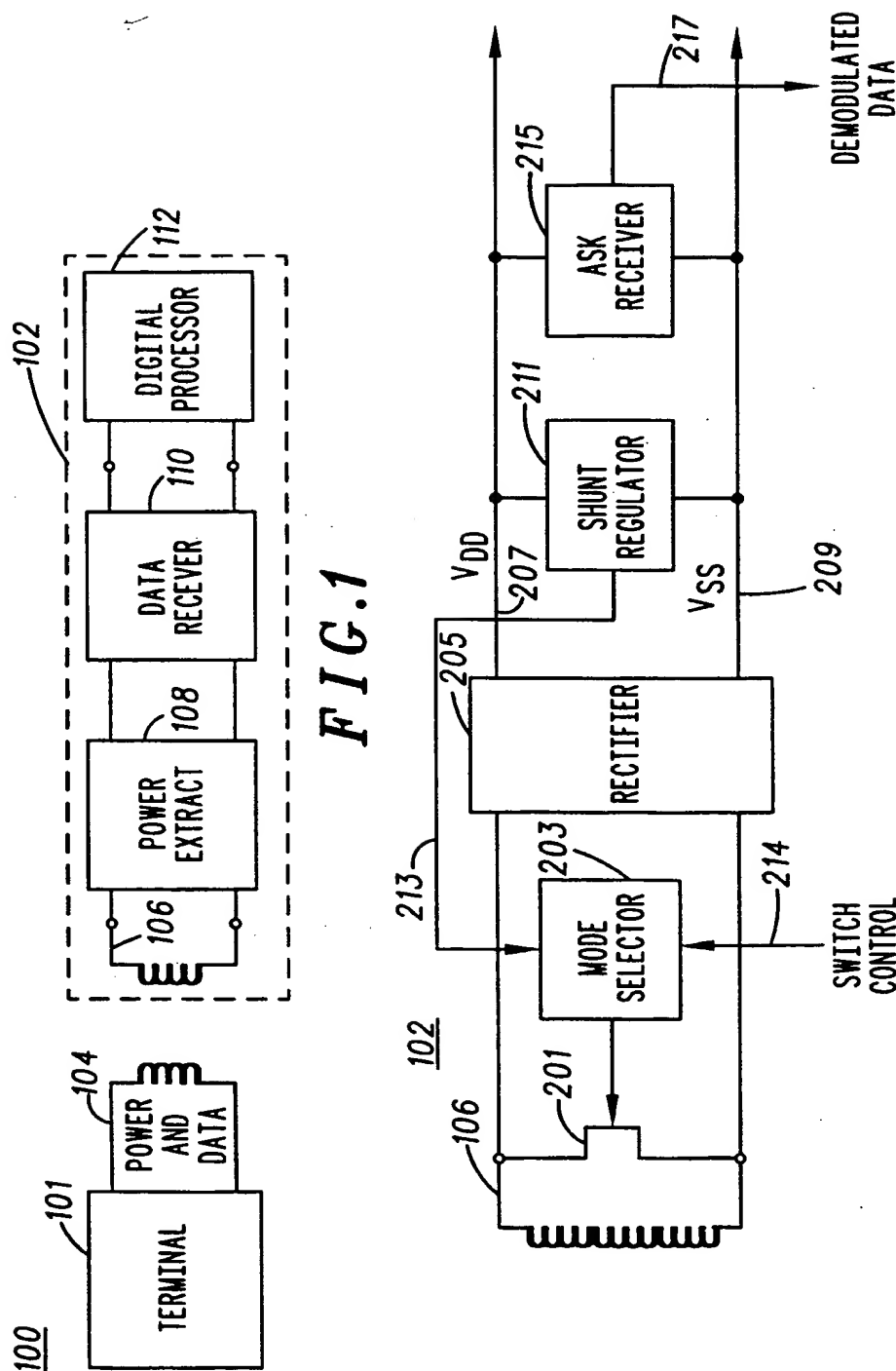
FIG.3

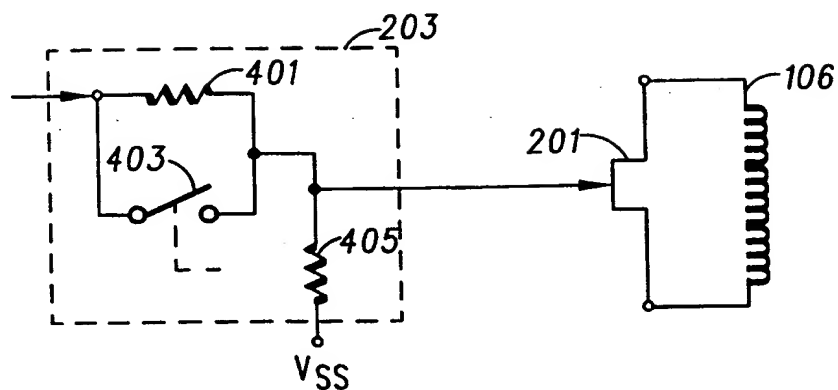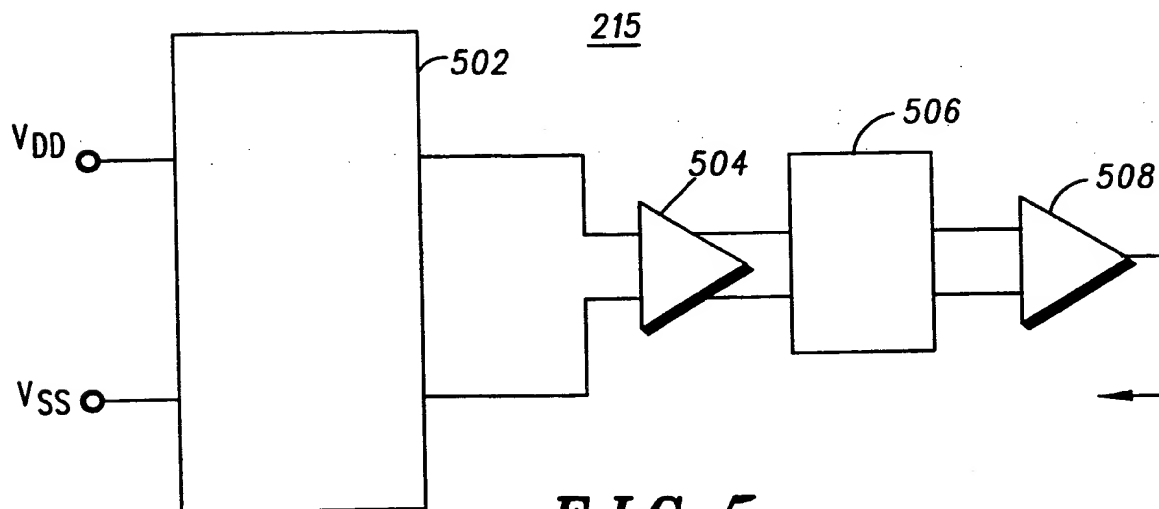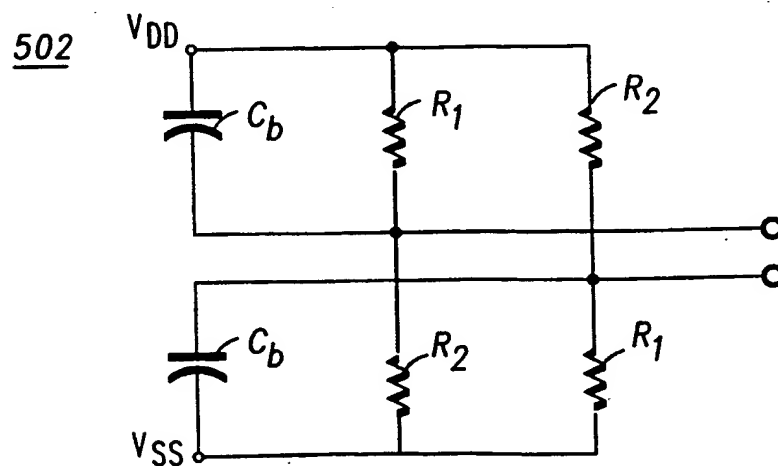*FIG.4*

FIG.5

FIG.6

SUBSTITUTE SHEET (RULE 26)
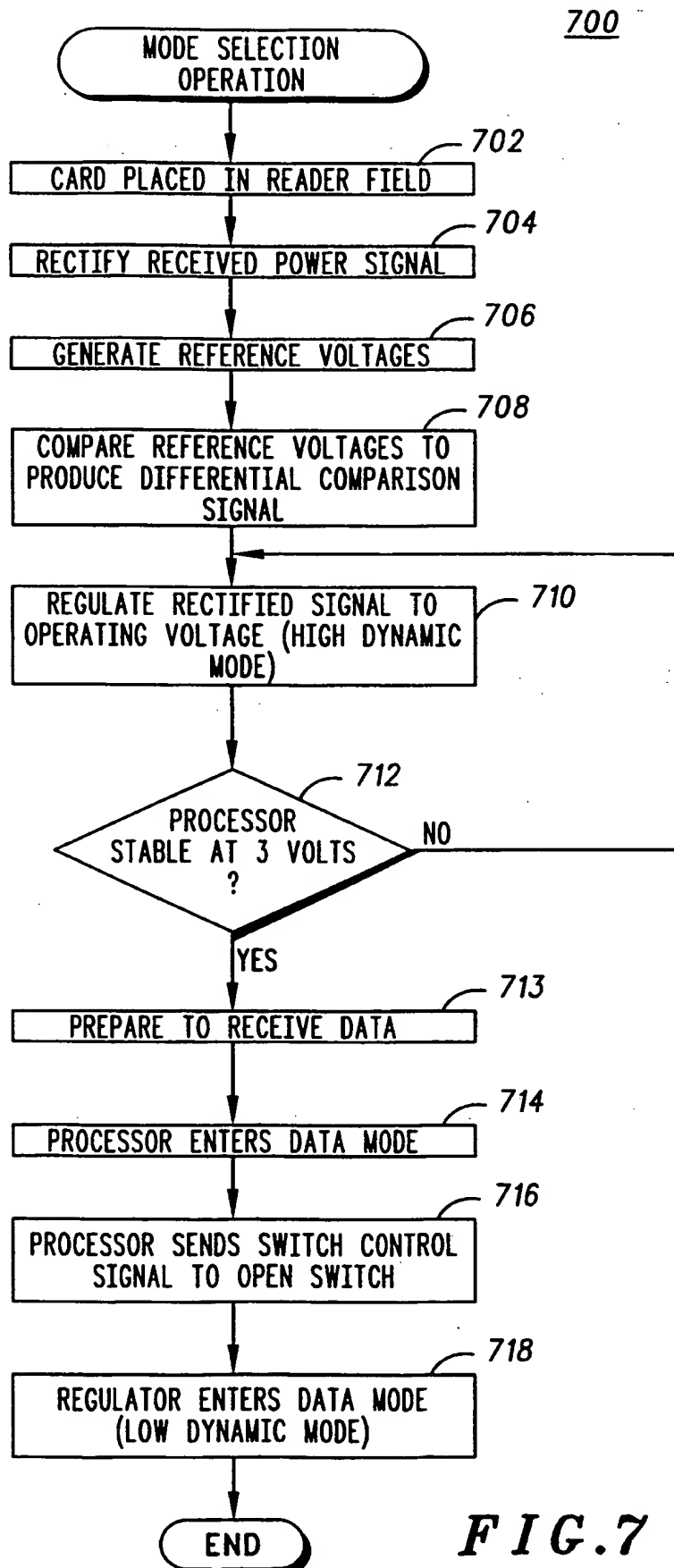
700

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        ╭─────────────────────────╮
        │    MODE SELECTION       │
        │     OPERATION           │
        ╰─────────────────────────╯
                    │
                    ▼
        ┌─────────────────────────┐  ╱702
        │ CARD PLACED IN READER FIELD │
        └─────────────────────────┘
                    │
                    ▼
        ┌─────────────────────────┐  ╱704
        │ RECTIFY RECEIVED POWER SIGNAL │
        └─────────────────────────┘
                    │
                    ▼
        ┌─────────────────────────┐  ╱706
        │ GENERATE REFERENCE VOLTAGES │
        └─────────────────────────┘
                    │
                    ▼
        ┌─────────────────────────┐  ╱708
        │ COMPARE REFERENCE VOLTAGES TO │
        │ PRODUCE DIFFERENTIAL COMPARISON │
        │         SIGNAL          │
        └─────────────────────────┘
                    │
                    ▼
        ┌─────────────────────────┐  ╱710
        │ REGULATE RECTIFIED SIGNAL TO │
        │ OPERATING VOLTAGE (HIGH DYNAMIC │
        │         MODE)           │
        └─────────────────────────┘
                    │
                    ▼
              ╱◇╲  712
        PROCESSOR            NO
    STABLE AT 3 VOLTS  ─────────►
         ?
              ╲◇╱
              │ YES
              ▼
        ┌─────────────────────────┐  ╱713
        │ PREPARE TO RECEIVE DATA │
        └─────────────────────────┘
                    │
                    ▼
        ┌─────────────────────────┐  ╱714
        │ PROCESSOR ENTERS DATA MODE │
        └─────────────────────────┘
                    │
                    ▼
        ┌─────────────────────────┐  ╱716
        │ PROCESSOR SENDS SWITCH CONTROL │
        │   SIGNAL TO OPEN SWITCH │
        └─────────────────────────┘
                    │
                    ▼
        ┌─────────────────────────┐  ╱718
        │ REGULATOR ENTERS DATA MODE │
        │    (LOW DYNAMIC MODE)   │
        └─────────────────────────┘
                    │
                    ▼
              ╭──────────╮
              │   END    │
              ╰──────────╯
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FIG.7

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :GO6K 19/06, 15/00, 15/02; GO6F 17/60; GO5F 1/10, 1/613
US CL : 235/ 492, 383, 384, 385, 351; 323/220, 222, 223
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

. U.S. : 235/ 492, 383, 384, 385, 351; 323/220, 222, 223

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
U.S. PTO APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,801,372 A (YAMAGUCHI) 01 September 1998 (01.09.98) see abstract and drawings.	1-15
Y	US 5,652,423 A (SAITOH et al.) 29 July 1997 (29.07.97), see abstract and figures.	1-15
A	US 5,326,965 A (INOUE) 05 JULY 1994 (05.07.94), see entire disclosure.	1-15
A	US 5,804,811 A (Saitoh et al) 08 September 1998 (08.09.98) see entire disclosure.	1-15
A	US 5,308,968 A (YAMAGUCHI) 03 MAY 1994 (03.05.94), see entire disclosure.	1-15

☐ Further documents are listed in the continuation of Box C.   ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier document published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 MARCH 1999	2 0 APR 1999

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